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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,865	12/29/2005	Thomas Maucksch	01012-1022	3967

7590 01/08/2008

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EXAMINER	
SUGLO, JANET L	
ART UNIT	PAPER NUMBER
2857	
MAIL DATE	DELIVERY MODE
01/08/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,865	MAUCKSCH, THOMAS	
	Examiner	Art Unit	
	Janet Suglo	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed April 18, 2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

2. The disclosure is objected to because of the following informalities: Page 9, lines 13-15 include "qchisq" which has not been defined or explained in the specification.

Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory

double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. **Claim 1** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. **Claim 2** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

6. **Claim 3** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. **Claim 4** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 3 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

8. **Claim 6** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended

use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

9. **Claim 7** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10. **Claim 8** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

11. **Claim 9** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 6 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

12. **Claim 10** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 7 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

13. **Claim 12** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 8 of copending Application No.

10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

14. **Claim 13** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 10 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

15. **Claim 16** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 13 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio

in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

16. **Claim 18** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 12 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

17. **Claim 19** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 11 of copending Application No. 10/513,909. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10,513,909 and a time delay error ratio in the instant application where the structure of Application 10,513,909 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

18. **Claim 1** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

19. **Claim 4** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of copending Application No. 10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

20. **Claim 6** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 3 of copending Application No. 10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended

use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

21. **Claim 7** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 of copending Application No. 10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

22. **Claim 10** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

23. **Claim 12** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 6 of copending Application No. 10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

24. **Claim 13** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 8 of copending Application No. 10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

25. **Claim 14** of provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim11 of copending Application No.

10/456,922. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are functionally the same method for the intended use of calculating a bit error ratio in Application 10/456,922 and a time delay error ratio in the instant application where the structure of Application 10/456,922 can be used to test the time delay ratio of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 101

26. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

27. **Claims 20-23** are rejected under 35 U.S.C. 101 because the claims are directed to neither a "process" nor a "machine," but rather embrace or overlap two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only. See MPEP 2173.05(p) Section II.

Claim Rejections - 35 USC § 112

28. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

29. **Claims 1-23** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "small" in claims 1, 2, 7, 8, 12, 13, 14, 16 and 17 is a relative term which renders the claim indefinite. The term "small" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

30. **Claim 3** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 3 uses the variable F_1 which has not been defined in either claim 3 or claim 1 which it is dependent upon.

31. **Claims 14 and 17** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 14 and 17 use the variable M which has not been defined.

32. **Claims 20-23** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 20-23 are single claims which claims both an apparatus and the method steps of using the apparatus and as such is indefinite under 35 U.S.C. 112, second paragraph. See MPEP 2173.05(p) Section II.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Deas et al. (US PGPub 2003/0014683) teaches a receiver with automatic skew compensation.

Malaney et al. (US PGPub 2002/0039349) teaches a telecommunications traffic regulator

Karlsson et al. (US Patent 6,167,039) teaches a mobile station having plural antenna elements and interference suppression.

Glista (US Patent 6,216,095) teaches automated in situ testing of railroad telemetry radios.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Janet Suglo whose telephone number is 571-272-8584. The examiner can normally be reached on Monday - Thursday from 6:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Janet L Suglo
January 3, 2008